Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph starting at page 1, paragraph number [0001], with the following rewritten paragraph:

[0001] This application is a division of Application No. 09/583,530, filed June 1, 2000, now ~~pending,~~ U.S. Patent No. 6,781,644, and based on Japanese Patent Application No. 11-154826, filed June 2, 1999, by Naoyuki Taguchi. This application claims only subject matter disclosed in the parent application and therefore presents no new matter.

Please replace paragraph starting at page 1, continuing on page 2, paragraph number [0004], with the following rewritten paragraph:

[0002] In this application, the drain pattern and the pixel electrodes are formed on a gate insulating layer shared between the thin film transistors of the pixels. The pixels are arranged in rows, and the pixel electrodes in each row are arranged at predetermined pitches. The pixel electrodes in a row are offset from the pixel electrodes in the next row by a half of the pitch. The pixels are laid [[on]] in what people call a "delta pattern." The array of thin film transistors laid [[on]] in the delta pattern has a drain pattern, a gate pattern and a storage pattern. These patterns are in proximity to one another, and are liable to [[he]] be short circuited and/or capacitively coupled to each other. Especially, when the array of thin film transistors includes [[the]] a pattern formed of amorphous silicon, residual amorphous silicon is liable to be left after the patterning step. The residual amorphous silicon ~~is causative of the~~ may cause a short-circuit between the drain pattern and the pixel electrode and/or between the adjacent pixel electrodes. If the residual amorphous silicon is left in the gap between the

delta drain pattern and the source pattern parallel to each other, ~~the~~ a short-circuit similarly takes place there between. ~~The~~ A short-circuit results in a point defect.

Please replace paragraph starting at page 2, paragraph number [0005], with the following rewritten paragraph:

[0003] If ~~the~~ patterns such as the drain lines and the pixel electrodes are spaced from each other, ~~the~~ a wide gap prevents the patterns from ~~the~~ a short-circuit. However, such a wide gap forces the designer to make the pixel electrodes narrower, and, accordingly, the aperture ratio is decreased. Moreover, the small aperture ratio results in a low transmittance of the screen. Thus, ~~the~~ a wide gap is not a good solution against ~~the~~ short-~~circuit~~ circuits due to the residual amorphous silicon and residual metal.

Please replace paragraph starting at page 2, continuing on page 3, paragraph number [0008], with the following rewritten paragraph:

[0004] There remains neither residual amorphous silicon nor residual alloy in the pattern shown in figure 4. However, a piece of residual amorphous silicon 14 and a piece of residual alloy 15 may be left on the pattern in the fabrication process as shown in figure 5. The piece of residual amorphous silicon 14 and the piece of alloy 15 ~~are causative of~~ may cause short-circuits. The Japanese Patent Publication of Unexamined Application teaches that the gate insulating layer 3 between the area assigned to the drain pattern 8 and the area assigned to the transparent pixel electrodes 9 is selectively etched away so as to form the contact slit 6.

Please replace paragraph starting at page 3, paragraph number [0010], with the following rewritten paragraph:

[0005] There is neither residual amorphous silicon nor residual alloy on the delta pattern shown in figure 9. However, a piece of amorphous silicon 14 and a piece of alloy 15 may be left on the delta pattern in the fabrication process as shown in figure 10. Even if the piece of residual amorphous silicon 14 and the piece of residual alloy 15 are left on the area between the drain pattern 8 and the transparent pixel electrodes 9 and/or the area between the adjacent transparent pixel electrodes 9, the piece of residual amorphous silicon 14 and the piece of residual alloy 15 are removed during the etching step, and the other example is prevented from ~~the~~ a short-circuit due to the piece of residual amorphous silicon 14 and the piece of residual alloy 15.

Please replace paragraph starting at page 4, paragraph number [0012], with the following rewritten paragraph:

[0006] The fabrication process for the second prior art liquid crystal display includes the step of forming the slit 16. Even if the piece of residual amorphous silicon 14 and the piece of residual alloy 15 are left on the area between the drain pattern 8 and the transparent pixel electrode 9 and/or the area between the adjacent transparent pixel electrodes 9, the piece of residual amorphous silicon 14 and the piece of residual alloy are etched away in the patterning step. Thus, the second prior art liquid crystal display is prevented from ~~the~~ a short-circuit due to the piece of residual amorphous silicon 14 ~~and/or~~ and/or the piece of residual alloy 15.

Please replace paragraph starting at page 4, paragraph number [0013], with the following rewritten paragraph:

[0007] The following ~~Following~~ problems are encountered in the above- described prior art liquid crystal displays. The contact slit 6 is a particular feature of the delta pattern of

the example of the first prior art liquid crystal display, and is formed around the pixel electrodes 9. The contact slit 6 extends between the drain pattern 8 and the pixel electrode 9, and is effective against the short-circuit therebetween due to the piece of amorphous silicon as shown in figure 5. However, the contact slit 6 can not prevent the drain pattern 8 and the source pattern 7 from ~~the~~ a short-circuit. This is because of the fact that the source pattern 7 extends in parallel to the drain pattern 8 without any contact slit 6 therebetween. As to the thin film transistors arranged in the delta pattern shown in figure 10, the storage pattern 12 is in parallel to the gate layer 2, and is liable to be short circuited with the gate layer 2 due to the piece of residual metal 15.

Please replace paragraph starting at page 4, continuing on page 5, paragraph number [0014], with the following rewritten paragraph:

[0008] The second prior art liquid crystal display is featured by the slit 16 formed in the protective dielectric layer 10. The slit 16 is also formed around the pixel electrode 9, and, accordingly, is effective against ~~the~~ a short-circuit between the drain pattern 8 and the pixel electrode 9 as shown in figure 15. However, the slit 16 can not prevent the drain pattern 8 and the source pattern 7 from ~~the~~ a short-circuit. Moreover, the slit 16 is terminated at the upper surface of the gate insulating layer 3, and can not prevent the gate layer 2 and the storage pattern 12 from ~~the~~ a short-circuit as similar to the other example of the first prior art liquid crystal display.

Please replace paragraph starting at page 5, paragraph number [0015], with the following rewritten paragraph:

[0009] Thus, both slits 6 and 16 can not perfectly prevent the conductive patterns 2/7/8/9/12 from short-circuit due to ~~the~~ a pieces of residual conductive material 14/15.

Please replace paragraph starting at page 5, paragraph number [0016], with the following rewritten paragraph:

[0010] It is therefore an important object of the present invention to provide a liquid crystal display which is free from ~~the~~ problems due to ~~the~~ pieces of residual conductive material.

Please replace paragraph starting at page 6, paragraph number [0020], with the following rewritten paragraph:

[0011] In accordance with another aspect of the present invention, there is provided a process for fabricating a liquid crystal display comprising the steps of preparing a substrate having a major surface, patterning a first conductive material layer into plural gate layers and plural storage electrode layers on the major surface, covering the plural gate layers and the plural storage electrode layers with a gate insulating layer, patterning an amorphous silicon layer into plural amorphous silicon layers on the gate insulating layer, ~~selectively~~ etching the gate insulating layer together with a piece of residual amorphous silicon connected between two of the plural amorphous silicon layers~~, if any,~~ for forming contact slits in the gate insulating layer, a piece of conductive material between one of the plural gate layers and an adjacent storage electrode layer being exposed to one of the contact slits~~, if any,~~ patterning a second conductive material layer into plural drain layers and plural source layers, the piece of conductive material being split during the pattering of the second conductive material layer, patterning a transparent material layer into pixel electrodes respectively held in contact with the plural source layers, and completing the liquid crystal display.

Please replace paragraph starting at page 9, paragraph number [0047], with the following rewritten paragraph:

[0012] Intrinsic amorphous silicon layers 4 are formed on the gate insulating layer 3, and heavily-doped n-type amorphous silicon layers 5 are laminated on both side areas of each intrinsic amorphous silicon layer 4. Source layers 7 and drain layers 8 are held in contact with the heavily-doped n-type amorphous silicon layers [[45]] 4 and 5, and the source layers 7 are spaced from the associated drain layers 8, respectively. Transparent pixel electrodes 9 are held in contact with the source layers 7, and the intrinsic amorphous silicon layers 4. The source layers 7, the drain layers 8, and the transparent pixel electrodes 9 are covered with a

protective dielectric layer 10. The gate insulating layer 3, storage electrode layers 12, and the associated transparent pixel electrodes 9 form in combination storage capacitors coupled to the pixels, respectively.

Please replace paragraph starting at page 10, paragraph number [0049], with the following rewritten paragraph:

[0013] The bent contact slit 13 is desirable from the aspect of not ~~to allow~~ allowing a piece of residual amorphous silicon and a piece of residual metal to form short-circuits between the conductive layers 2 and 8 and/or 8 and 12. Even if a piece of residual amorphous silicon was left over the gate layer 2 and the drain layer 8, a part of the piece of residual amorphous silicon is etched away together with a piece of gate insulating layer 3 while a kind of etchant is forming the bent contact slits 13 in the gate insulating layer 3. After the formation of the bent contact slits 13, the drain layers 8 are patterned. Even if a piece of residual metal was left between the gate layer 2 and the storage electrode layer 12, a part of the piece of residual metal is exposed to the bent contact slit 13, and is etched away in the etching step for the drain layers 8. Thus, the piece of residual amorphous silicon is split into pieces of residual amorphous silicon in the patterning step for the bent contact slit 13, and the piece of residual metal is split into pieces of residual metal in the patterning step for the drain layers 8. This results in that the bent contact slits 13 are effective against short-circuit between the gate layer 2 and the drain layer 8 and short-circuit between the gate layer 2 and the storage electrode layer 12. The bent contact slit 13 is the combination of the slit in the previous stage and the slit in the next stage, and, accordingly, pieces of residual amorphous silicon on most area are split in the etching step. Pieces of residual metal are always exposed to the bent contact slits 13, and are split in the patterning step for the drain layers 8.

Please replace paragraph starting at page 12, paragraph number [0056], with the following rewritten paragraph:

[0014] As will be understood from the foregoing description, the bent contact slits 13 are effective against the short-circuit between the source layers 7 and the drain layers 8 and between the gate layers 2 and the storage electrode layers 12. A piece of residual amorphous

silicon 14 is liable to be left during the patterning step for the heavily-doped n-type amorphous silicon layers, and a piece of' residual metal 15 is left during the patterning step for the gate/storage electrode layers 2/12 (see figure 20). Even so, while the bent contact slits 13 are being formed in the gate insulating layer 3, the piece [[of]] residual amorphous silicon 14 is split into pieces, and the piece of residual metal 15 is exposed to the bent contact slit 13. The piece of residual metal 15 is also broken during the patterning step for the source/drain layers 7/8. Thus, the bent contact slits 13 are effective against the short-circuit.